

**MARC 2023**  
**Palacios Group Abstracts**

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David Morales Loro  
damorale@mit.edu

Chamber design of a portable breathalyzer for disease diagnosis.

D.Morales, M. Xue, T.Palacios

**Sponsorship:** NSF CIQM

Our group has built a graphene-based sensor array that can accurately measure the concentration and type of different chemicals of interest. In this project, we are developing a chamber design that will allow to use this sensor as a portable breathalyzer for disease diagnosis. This system could provide a non-invasive, cheap and fast approach for disease diagnosis. Although significant research has been made in this field over the years, none has focused on the optimal design of the chamber of these devices, which has to optimize the contact between the sensors and the air samples and address problems such as moisture, velocity control of air, recirculation and turbulences. Our work studies the airflow properties in different chamber models and, with the help of simulations and experiments with the actual analysis sensors, attempts to create a reusable in-situ breath analyzer design. These results will help develop devices that will be used in clinical trials and that, in the future, could be used for diagnosis of diabetes, Parkinson and other conditions.

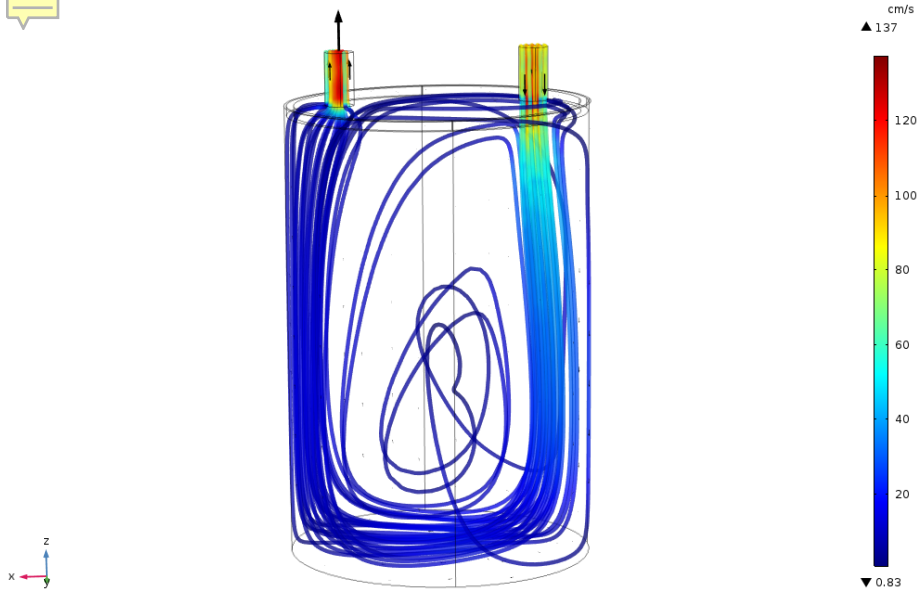


Figure 1: airflow and velocity profile simulations in one of the models

James Greer  
greerj@mit.edu

### p-GaN/AlGaN Selective Etch Process for p-GaN-Gated AlGaN/GaN HEMTs

J. A. Greer, M. Yuan, Q. Xie, J. Niroula, T. Palacios

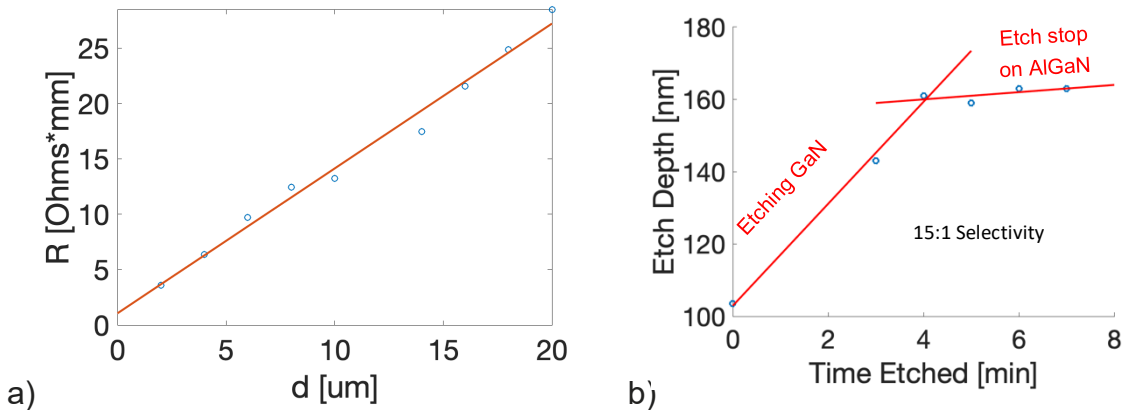
**Sponsorship:** ExxonMobil through MIT Energy Initiative UROP program, MIT.nano, Lockheed Martin Corp (Grant No. 025570-00036)

p-GaN-gated AlGaN/GaN HEMT is a promising technology for applications in E/D-mode high temperature (500°C+) digital logic and power electronics due to its significantly improved voltage swing, noise margin, and gain over traditional semiconductor devices. A crucial step in the fabrication of these devices is the p-GaN/AlGaN selective etch process, which requires high uniformity, high selectivity, and low etch-induced damage.

In this work, an etch process to selectively etch p-GaN over AlGaN using an SF<sub>6</sub> and BCl<sub>3</sub> chemistry was demonstrated. Etch stop was achieved after 4 minutes along with a p-GaN/AlGaN selectivity of 15:1 (Figure 1b). After depositing ohmic contacts, a contact resistance of 0.52 Ohm\*mm and sheet resistance of 1307 Ohm/square was measured. These results enable the fabrication of enhancement-mode GaN transistors with excellent uniformity and transport properties.

(Figure 1a).

4 probe TLM measurements. b) Etch depth vs Etch time



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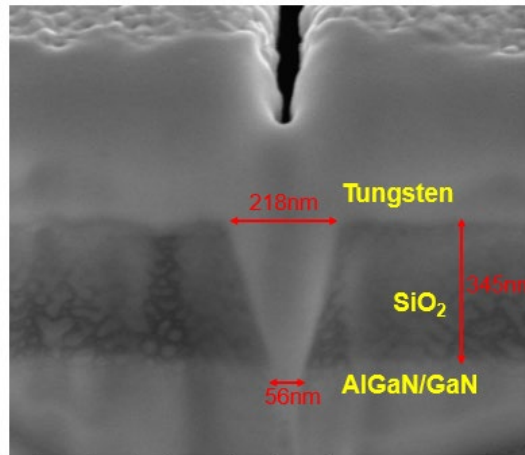
John Niroula  
jniroula@mit.edu

High Temperature RF GaN electronics. J. Niroula, Q. Xie, P. Yadav, T. Palacios

**Sponsorship:** AFOSR (Grant No. [FA9550-22-1-0367](#)), [Lockheed Martin](#)

High temperature electronics has received much interest recently due to emerging applications in geothermal well exploration, hypersonic flight electronics, and space exploration. GaN based devices are an exciting contender for extremely high temperature environments due to their high mobility, high saturation velocity, especially beyond 250°C, which is the limit of traditional silicon based devices. In this project we aim to develop a high performing GaN based RF device that operates at both room temperature as well as 500°C. Here we use tungsten as the gate metal because of its refractory nature and ability to robustly withstand high temperature environments. However, since Tungsten cannot be easily lifted off, so we have developed an SiO<sub>2</sub> etchback and Tungsten fill to define our gate electrode (Figure 1) and make it a T-gate process.

Figure 1: Focus Ion Beam cross-sectional image of a high temperature GaN transistor, showing excellent gate height to gate length ratio



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Joshua Perozek  
jperozek@mit.edu

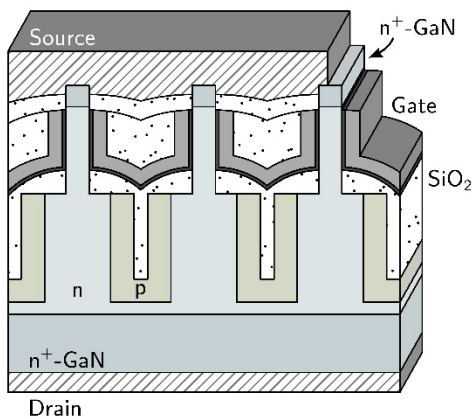
## Vertical GaN Superjunction Transistors

J. Perozek, M./ T. Palacios (who all should be included?)

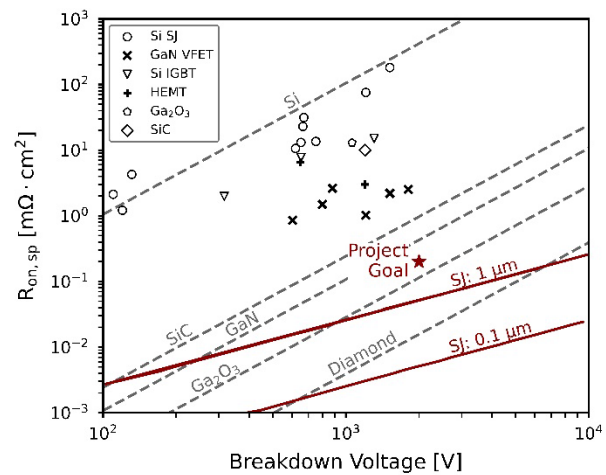
Sponsorship: ARPA-E 2021 OPEN Project (Grant No. DE-AR0001591)

Increasing sustainable energy practices have spurred the need for next generation power conversion systems. At their core, these systems, which are essential for solar farms, data centers, and electric vehicles, require small, fast, and affordable power transistors. While gallium nitride (GaN) as a material is uniquely suited for these applications, existing transistors are far from reaching their theoretical limits. The inability to optimize the electric fields within the device has prevented commercial transistors from achieving the performance promised by theoretical studies.

In this work, we aim to use our expertise in fabricating vertical GaN FinFETs to surpass the unipolar limit and create the first GaN superjunction transistors. These transistors use alternating n- and p-type regions to optimize the electric field profile within the transistor to reach the theoretical limits of semiconductor performance. Such devices could outperform existing tech by 50-100× and significantly improve energy conversion efficiency.



(a)



(b)

(a) Schematic of a vertical GaN superjunction transistor and (b) ultimate performance limits for GaN superjunctions of various pitches benchmarked against several semiconductors and actual devices.

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Nishat Fahmida Protyasha  
protya@mit.edu

Robust High Temperature GaN Device Characterization and Simulation  
Framework  
N. Protyasha, J. Niroula, P. Yadav, Q. Xie, T Palacios  
**Sponsorship:** [MIT SuperUROP Program]

Wide band semiconductors such as SiC and Gallium Nitride (GaN) are ideal for building electronics suitable for extremely high temperature applications such as deep well oil drilling, hypersonic aircrafts, and the exploration of Venus. However, there is a critical lack of understanding of these devices at these high temperatures. In this project, we use the MIT Virtual Source GaN FET (MVSG) compact model as the foundation to develop a robust experimental and modeling framework for the characterization and simulation of AlGaN/GaN High Electron Mobility Transistor (HEMT) devices across a wide range of temperatures ranging from 25°C to 500°C. Multitude of measurement techniques including DC-IV, pulse-IV, C-V, S-parameter measurements are performed to extract physical device parameters, which are then analyzed to understand physical mechanisms limiting device performance at high temperature.

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Pao-Chuan Shih  
pcshih@mit.edu

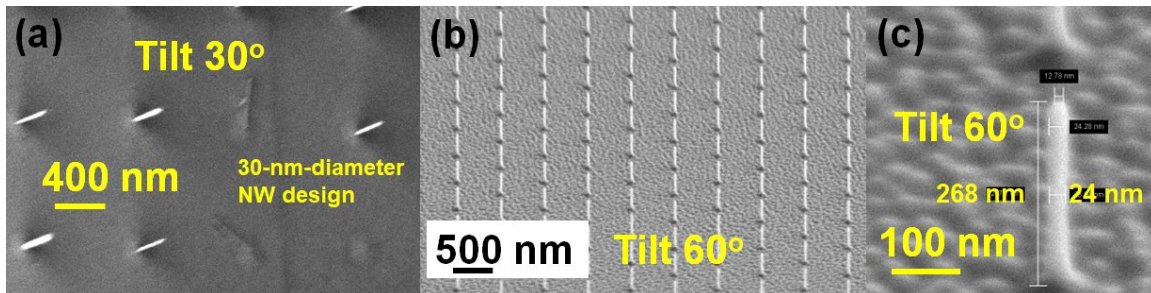
Uniform High-Aspect-Ratio GaN Vertical Sub-30-nm-Diameter Nanowires  
Formed by Optimized Two-Step Etching Process

P.-C. Shih and T. Palacios

**Sponsorship:** AFOSR through MURI Empty State Electronics Project  
(Grant No. 028311-00005)

III-Nitride semiconductors are key enablers of many applications, including optoelectronics, power electronics, and RF amplifiers. However, so far, III-Nitride vertical structures with sub-100 nm dimensions still face yield and uniformity issues, limiting III-Nitrides' impact in nanostructure devices and product. In this project, we optimized the etching process for GaN, and combine it with the subsequent wet-based digital etching (DE) to demonstrate uniform and high-yield GaN sub-30-nm-diameter vertical nanowires (NWs) with high aspect-ratio (> 12:1). We are currently investigating the effects of this approach on material damage and device defects. This new technology is expected to advance future development on III-Nitride nanoelectronics and optoelectronics, for example, vertical NWs for water splitting (for fuel generation) and vertical NW transistors.

Tilted SEM images of GaN vertical NWs formed by (a) dry etching and conventional TMAH treatment and (b) (c) the optimized dry etching with DE. There are uniformity and yield issues in NWs shown in (a), while the NWs shown in (b) are more uniform.



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Pradyot Yadav  
yadavps@mit.edu

Heterogeneous Integration of GaN and Si for MMICs above 300 GHz, 6G Applications and Beyond

P. Yadav

**Sponsorship:** AFOSR (Grant No. FA9550-22-1-0367) and Lockheed Martin Corporation (Grant No. 025570-00036)

The future of Gallium Nitride (GaN) radio frequency (RF) circuit technology is at the intersection of material science, physical modelling, and circuit design. Currently, these are three separate fields with little-to-no communication between them, resulting in critical limitations to today's technology. There is an urgent need for these fields to collaborate, cross-pollinate, and intersect in order to modernize and advance innovation for the next generation of RF circuits.

To design the most efficient RF and mmWave circuits, we must embrace an interdisciplinary approach, as described in fig. 1, that combines new GaN transistors with engineered linearity, novel heterogeneous integration with state-of-the-art Silicon (Si) control circuits, and advanced physics-based modeling. This project sets the foundation of the next generation of RF and mixed signal circuits for applications such as 6G and the extreme environments of hypersonic vehicles.

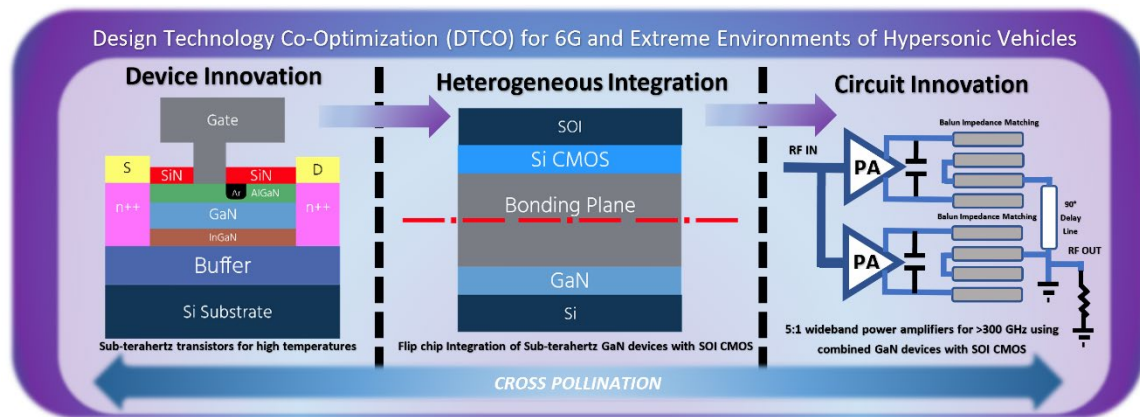


Figure 1 Plan for development of novel transistors and high frequency, wideband power amplifiers targeting the >300 GHz Spectrum with heterogeneous integration of GaN and CMOS



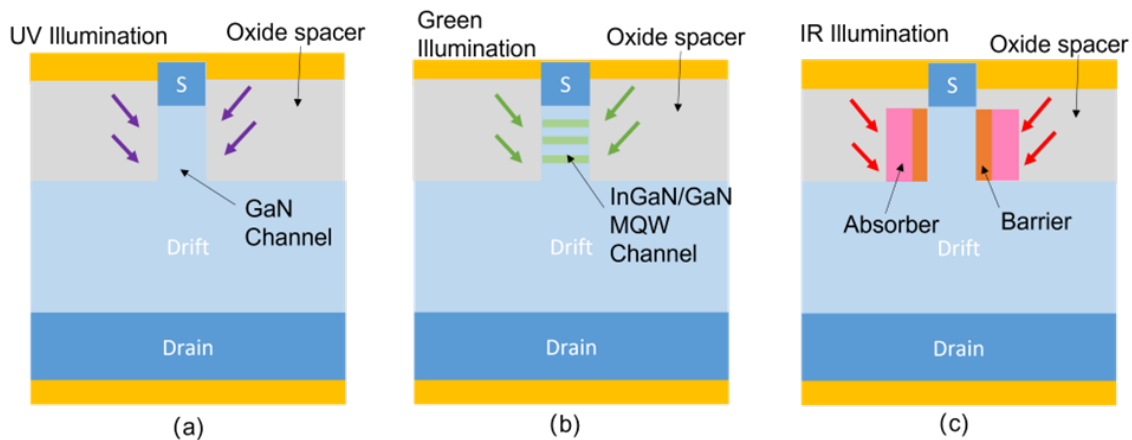
Jung-Han Hsia  
 jhsia@mit.edu

Optically Controlled Vertical GaN Power finFETs

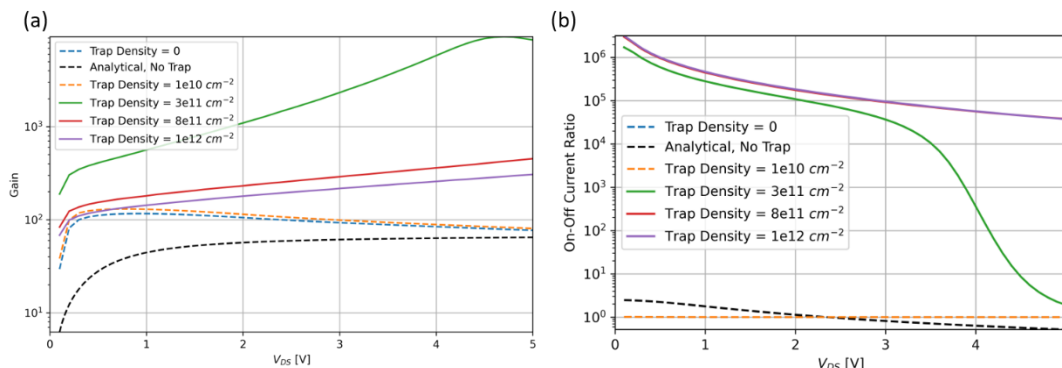
Jung-Han Hsia, Kevin Limanta, Josh Perozek, Richard Molnar and Tomás Palacios

**Sponsorship:** Office of Naval Research ([Grant No. N00014-22-1-2468](#))

In recent years, the boost in consumer electronics, automotives and data centers has increased the electricity demand. The delivery and transformation of power through electric grids require many efficient power converters and electronics that can withstand high current and voltages. However, traditional power electronics are mostly electrically triggered, which can complicate the circuitry design and cause electromagnetic interference (EMI). The use of optically triggered devices will simplify the circuitry design, reduce EMI and potentially increase the operating frequency. Although optically triggered silicon devices have already been developed, there are however no demonstrations on optically controlled GaN power transistors [1]. In this project, we are evaluating the performance of several optically-controlled GaN transistors as shown in Figure 1. This poster will present the design space of different approaches identified through initial simulations, as shown in Figure 2.



**Figure 1.** Approaches for optically triggered devices (a) Directly-triggered UV finFET with GaN channel (b) Directly-triggered blue/green finFET with embedded InGaN/GaN MQWs (c) Absorber-coupled finFET



**Figure 2.** Simulated (a) gain and (b) on-off ratio for ungated GaN finFET with different sidewall trap density

**References:**

[1] Zhang, Y., Sun, M., Perozek, J., Liu, Z., Zubair, A., Piedra, D., . . . Palacios, T. (2018). Large area 1.2 kv gan vertical power finfets with a record switching figure-of-merit. IEEE Electron Device Letters, 1-1. doi:10.1109/led.2018.2880306

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Minsik Oh  
oms9585@mit.edu

Use of Ion Implantation to Engineer the Electric Field Profiles in GaN Superjunction Devices

M. Oh, J. Perozek, J. Hsia, and T. Palacios

**Sponsorship:** “ARPA-E”, “Ericsson”

Power electronic devices play a significant role in various applications such as power grids and electric vehicles. Power devices are required to block high voltages while having a low resistance to reduce power consumption during operation. In this context, Gallium Nitride (GaN) is highly promising due to its wide bandgap and excellent transport parameters compared to other semiconductors such as Si. Additionally, superjunction structures consisting of alternating n- and p-type columns have significantly improve the performance of Si-based power devices, since they can overcome the limitation on the trade-off between high breakdown voltage and low ON resistance that 1-D unipolar devices have. However, GaN vertical superjunction devices have never been reported so far due to the difficulties in the epitaxial growth and fabrication.

In this work, the feasibility of fabricating GaN superjunction devices through ion implantation is explored through simulation. Stopping and Range of Ions in Matter (SRIM) is used to acquire the estimated Si doping profiles in p-GaN substrate for several sets of ion implantation parameters, and Technology Computer Aided Design (TCAD) simulation is conducted with the doping profiles from SRIM to verify the 2-D electric field profiles in the superjunction structure. Finally, the technical challenges that are not considered in the simulation are discussed.

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hw93528@mit.edu

High Performance P-type 2D Transistors with Low Resistance Contacts  
Hae Won Lee, Jiadi Zhu, Ji-Hoon Park, Yaseen Hou, Jagadeesh S. Moodera,  
Jing Kong and Tomas Palacios  
**Sponsorship:** Intel (ISRA)

Among all the emerging materials, two-dimensional (2D) semiconductors appear to be promising for the next generation electronics due to their atom layer thickness, relatively wide band gap and high mobility. Whereas numerous research has been focused on n-type 2D semiconductors, e.g. molybdenum disulfide ( $\text{MoS}_2$ ), in the past decades, p-type 2D materials, e.g. tungsten diselenide ( $\text{WSe}_2$ ), have not been explored sufficiently, which have equal importance in building 2D complementary metal-oxide-semiconductor (CMOS) circuits. In particular, reducing the contact resistance between a p-type 2D channel and a metal contact to a silicon transistor-comparable level is essential to achieve a high-performance p-type transistor.

In this work, we demonstrate a high-performance p-type  $\text{WSe}_2$  transistor with platinum (Pt) contacts. Monolayer  $\text{WSe}_2$  film is directly synthesized on  $\text{SiO}_2/\text{Si}$  substrate using metal organic chemical vapor deposition (MOCVD). Pt contacts are sequentially formed with molecular beam epitaxy (MBE) technique, at a high vacuum level ( $3 \times 10^{-10}$  Torr). This allows an ultra-clean interface between the  $\text{WSe}_2$  and Pt, which results in low contact resistance. Moreover, we analyze the quality of contacts formed at different pressure levels by two different methods, i.e. using MBE and conventional electron beam evaporation ( $10^{-6} \sim 10^{-7}$  Torr). This research on high-performance p-type 2D transistor with reduced contact resistance will be an important step for the using 2D materials in CMOS circuits. For future work, we will expand our research on ohmic contact by exploiting semi-metal contacts which can reduce metal-induced gap states (MIGS) between semiconductors and contact materials.

Qingyun Xie  
[gyxie@mit.edu](mailto:gyxie@mit.edu)

### Monolithically Integrated Gallium Nitride Complementary Technology for All-GaN Multi-Functional Chips

Q. Xie, J. Niroula, P. Yadav, M. Yuan, N. Chowdhury, T. Palacios

**Sponsorship:** Samsung Electronics Co., Ltd. (award no. 033517-00001)

Qualcomm, Inc. (award no. MAS-492857)

Intel Corp. (award no. 027196-00001)

The rising performance of GaN power ICs has offered compactness, and record levels of efficiency and power for data centers, power adapters, electric vehicles (EVs), and 5G telecommunication systems. However, the lack of a practical GaN p-FET introduces major limitations: (1) significant static power dissipation (resulting from the use of n-type enhancement-mode/depletion-mode logic); (2) a roadblock towards all-GaN integration (e.g. control loops, analog mixed-signal blocks). Furthermore, the availability of high-side switching GaN p-FETs would circumvent the switching speed bottleneck (limited common-mode transient immunity (CMTI) in the level shifter), therefore enabling more efficient power converters.

In recent years, extensive research has been pursued at MIT in the emerging domain of GaN complementary technology, which features: (1) integration of p-FET and n-FET on the same platform without the need of regrowth of III-N material; (2) scalable platform for eventual commercialization; (3) ability to withstand the large heat generation in EVs, data centers, and base stations; (4) high p-FET and n-FET performance. The reported progress has been enabled by a combination of new device structures (e.g. self-aligned p-FinFET) and process optimization (e.g. techniques to reduce etch-induced damage). Current research effort is focused on advancing device-level performance and exploration of novel GaN complementary circuits.

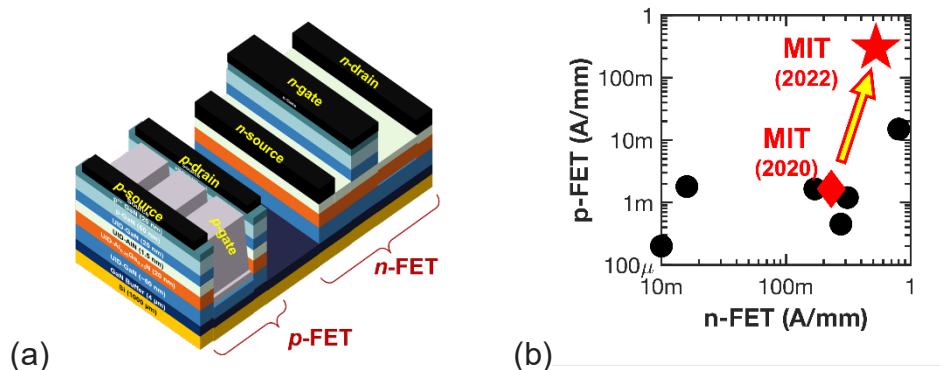


Figure: (a) Highly-scaled GaN complementary technology on GaN-on-Si substrate; (b) advancement in the performance of monolithically integrated n-FET



and p-FETs reported in the literature, as exemplified by their current densities over the years.

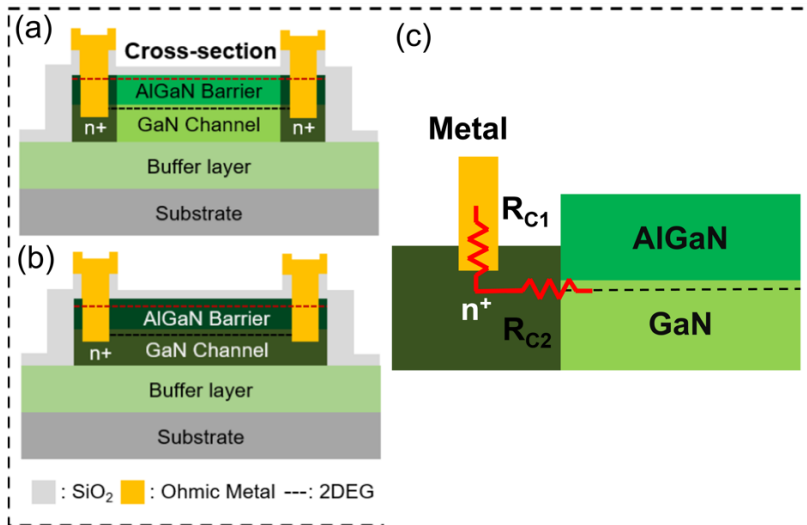
Qingyun Xie  
[gyxie@mit.edu](mailto:gyxie@mit.edu)

Si-Ion Implanted Ohmic Contact Technology for GaN-on-Si HEMTs  
M. Yuan, Q. Xie, J. Niroula, M. Oh, P. Yadav, N. Chowdhury, T. Palacios  
**Sponsorship:** National Aeronautics and Space Administration (NASA) (grant no. 80NSSC17K0768) Lockheed Martin Corp. (grant no. 025570-00036)  
Air Force Office of Scientific Research (AFOSR) (grant no. FA9550-22-1-0367)  
Advanced Research Projects Agency-Energy (ARPA-E) ([Grant No. DE-AR0001591](#))

A scalable and manufacturable process technology for ohmic contacts is critical for the realization of highly integrated GaN electronics. Considering the aggressive scaling commonly found in high-speed GaN transistors, low contact resistance becomes increasingly significant (over channel resistance). Among the methods of formation of ohmic contacts to the AlGaN/GaN channel, including direct alloying of metal stack, regrowth of  $n^+$  GaN regions, and ion implantation to form  $n^+$ -GaN regions, the latter stands out thanks to its good surface morphology, edge roughness, and the ability to support metallization of refractory metals which is desired for high temperature applications. Early research efforts have focused on ion implanted contacts in AlGaN/GaN-on-SiC which require excessively high annealing temperatures ( $>1300$  °C). The rapid proliferation of GaN RF and power electronics in recent years call for research into a robust Si-ion implanted process technology on the scalable (up to 12 in.) GaN-on-Si platform.

This work provides a comprehensive evaluation of the Si-ion implanted contact technology for GaN-on-Si HEMTs. By optimizing the implantation dose, energy, annealing temperature and ohmic recess depth, a low contact resistance of  $0.3 \Omega \cdot \text{mm}$  was achieved. The proposed contact scheme shows high tolerance on ohmic recess, compatibility with different metal stacks, and smooth surface morphology. To the best of the authors' knowledge, the proposed contact technology yields the lowest contact resistance in ion implanted-AlGaN/GaN ohmic contacts at the lowest annealing temperature. The results were obtained, for the first time, using AlGaN/GaN on Si (instead of SiC) substrate, therefore offering significant promise for Si-ion implanted contacts in GaN-on-Si HEMTs.

The authors gratefully acknowledge Applied Materials, Inc. for the provision of ion implantation facilities.



(a) Cross-section of the Si-ion implanted ohmic contact proposed in this work. (b) All-area implanted reference structures. (c) Analysis of the resistance components in the proposed ohmic contact.

Hridibrata Pal  
hpal@mit.edu

High-power AlGaIn finFET for mm-Wave applications  
Hridibrata Pal, Pao-Chuan Shih, Tomas Palacios  
**Sponsorship:** ARO

High frequency electronics is becoming increasingly important for today's commercial, military and space communication needs. To enable the mm-Wave 5G network, power amplifiers need to provide high power density, gain, efficiency and linearity; but the performance of state-of-the-art GaN HEMTs is limited for frequencies  $> 30$  GHz. AlGaIn is an UBWG material that has a 3-5 times higher Johnson's Figure of Merit (JFOM) compared to GaN due to its much higher breakdown electric field ( $> 8$  MV/cm). Therefore, AlGaIn devices have the potential to surpass the state-of-the-art GaN HEMTs and achieve an order of magnitude higher power density at frequencies  $> 90$  GHz as well as better linearity and efficiency at lower frequencies.

In this project, we propose to leverage the superior material properties of high-Al content ( $> 50\%$ ) AlGaIn to fabricate a finFET with fins of aspect-ratio ( $H_{fin}/W_{fin}$ )  $> 20:1$ . The tall fin structure increases the effective width of the channel and hence would lead to a higher current density and power density.

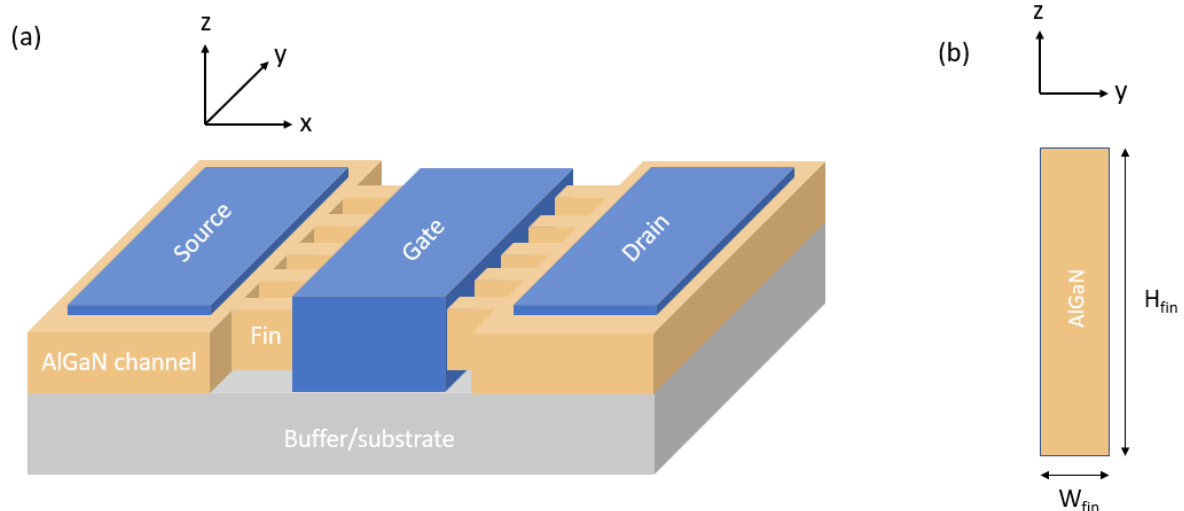


Figure 3. (a) Schematic of the proposed AlGaIn finFET. (b) Cross-section of the fin, target  $H_{fin} > 2 \mu\text{m}$ .