MARC 2023
Palacios Group - Pitch Presentations

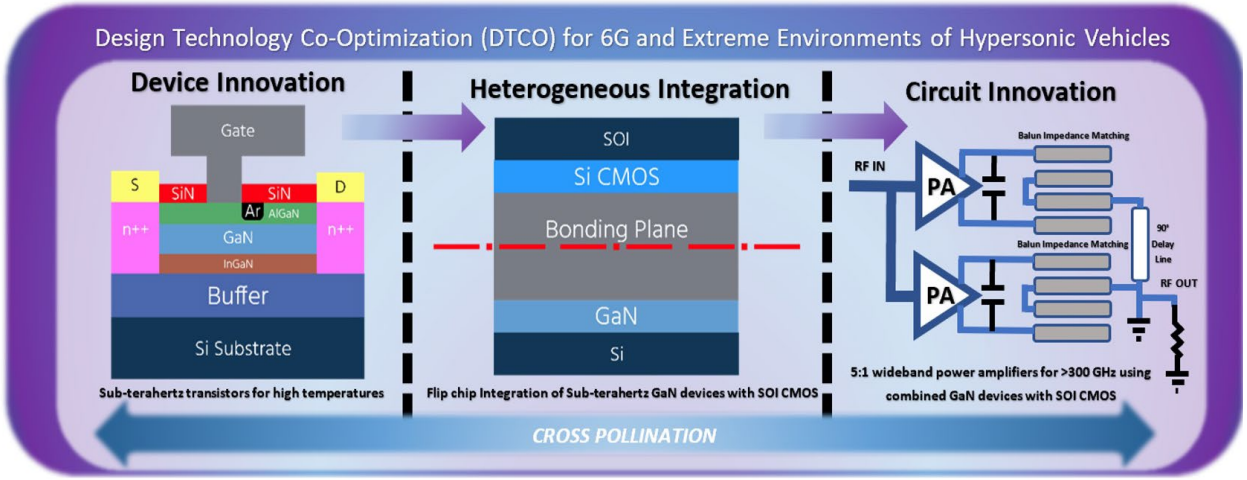
January 20th, 2023

MARC 2023
Palacios Group - Pitch Presentations

1. Pradyot Yadav
2. Qingyun Xie
3. Hae Won Lee
4. Pao-Chuan Shih
5. Jung-Han Hsia (Sharon)
6. David Morales
7. Gillian Micale
8. Jiadi Zhu
9. Minsik Oh
10. Joshua Perozek
11. Hridibrata Pal
12. John Niroula

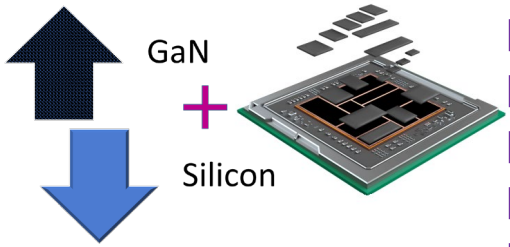
Heterogeneous Integration of GaN and Si for MMICs above 300 GHz, 6G Applications and Beyond

Pradyot Yadav, Q. Xie, J. Niroula, T. Palacios



Satellite

Radio Astronomy



Heterogeneous Integration

Security Screening

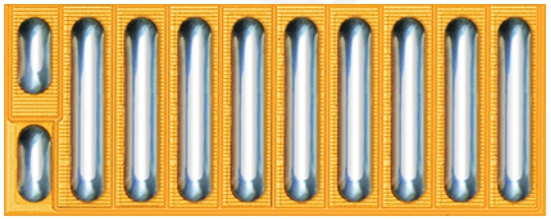
Automotive Radar

6G

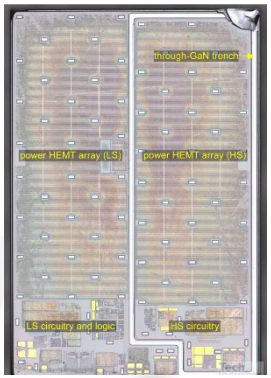
Cellular

Monolithically Integrated GaN Complementary Technology for All-GaN Multi-Functional Chips

Qingyun Xie, N. Chowdhury, M. Yuan, J. Niroula, P. Yadav, T. Palacios



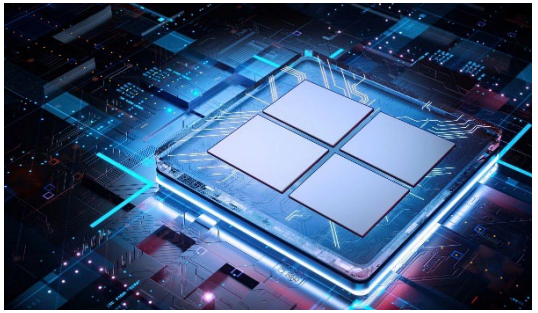
2014

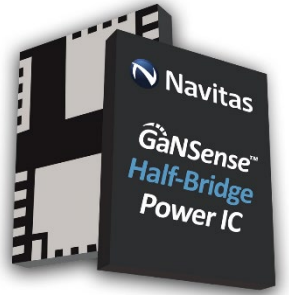


EPC

EPC2152

(2020)





Navitas

NV6247

(2022)

intel

Intel's Vision 2030

(IEDM2022)

E-mode transistor

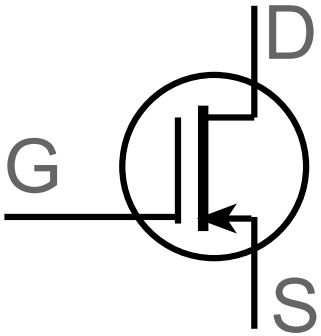
Integrated circuits (half bridge and gate driver) < 100 transistors

Acknowledgments:
Intel Corp. (027196-00001)
NASA (80NSSC17K0768)
Samsung Electronics Co., Ltd. (033517-00001)
Qualcomm Inc. (MAS-492857)
ARPA-E (AR0001591)

Monolithically Integrated GaN Complementary Technology for All-GaN Multi-Functional Chips

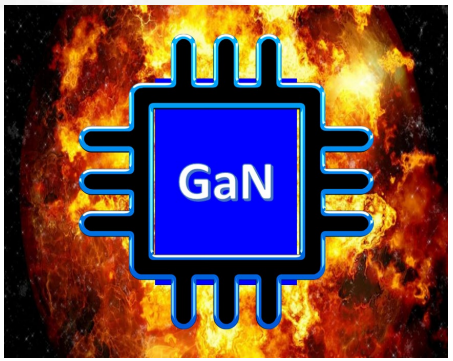
Qingyun Xie, N. Chowdhury, M. Yuan, J. Niroula, P. Yadav, T. Palacios

GaN CMOS = Monolithically integrated GaN *n* + *p*-FET + Superior properties of GaN for power and RF



GaN p-channel transistor

Applications in power, analog mixed-signal



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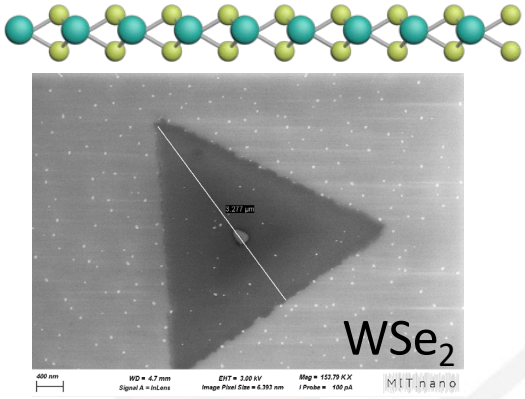
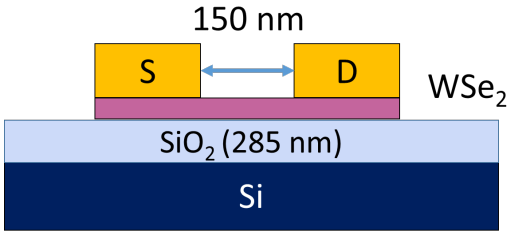
ARPA-E (AR0001591)

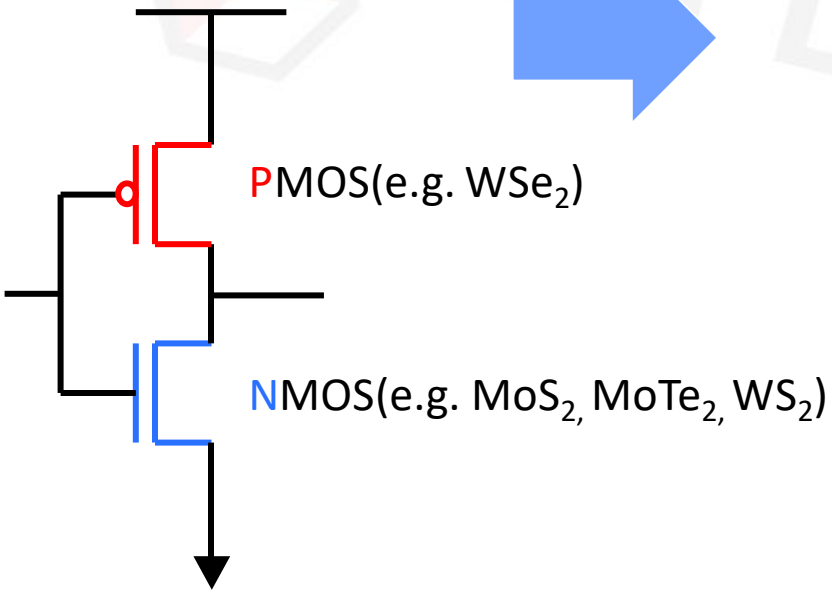
High Performance P-type 2D Transistors with Low Resistance Contacts

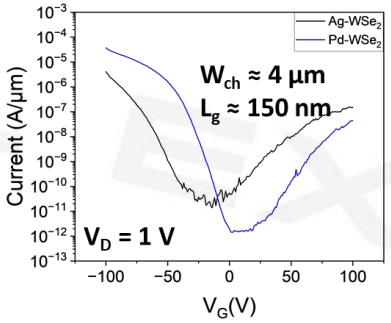
Hae Won Lee, Jiadi Zhu, Ji-Hoon Park, Yasen Hou, Jagadeesh S. Moodera, Jing Kong and Tomás Palacios

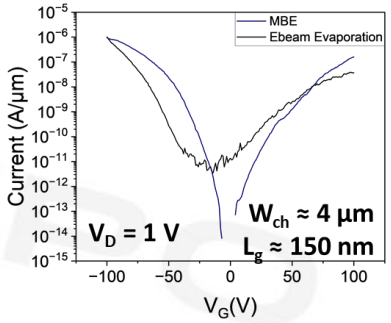


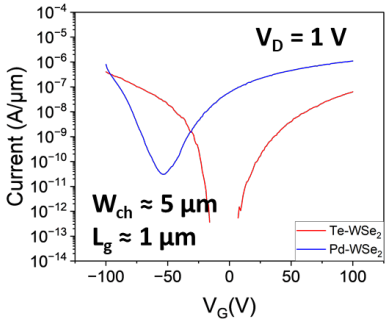
P-type 2D device







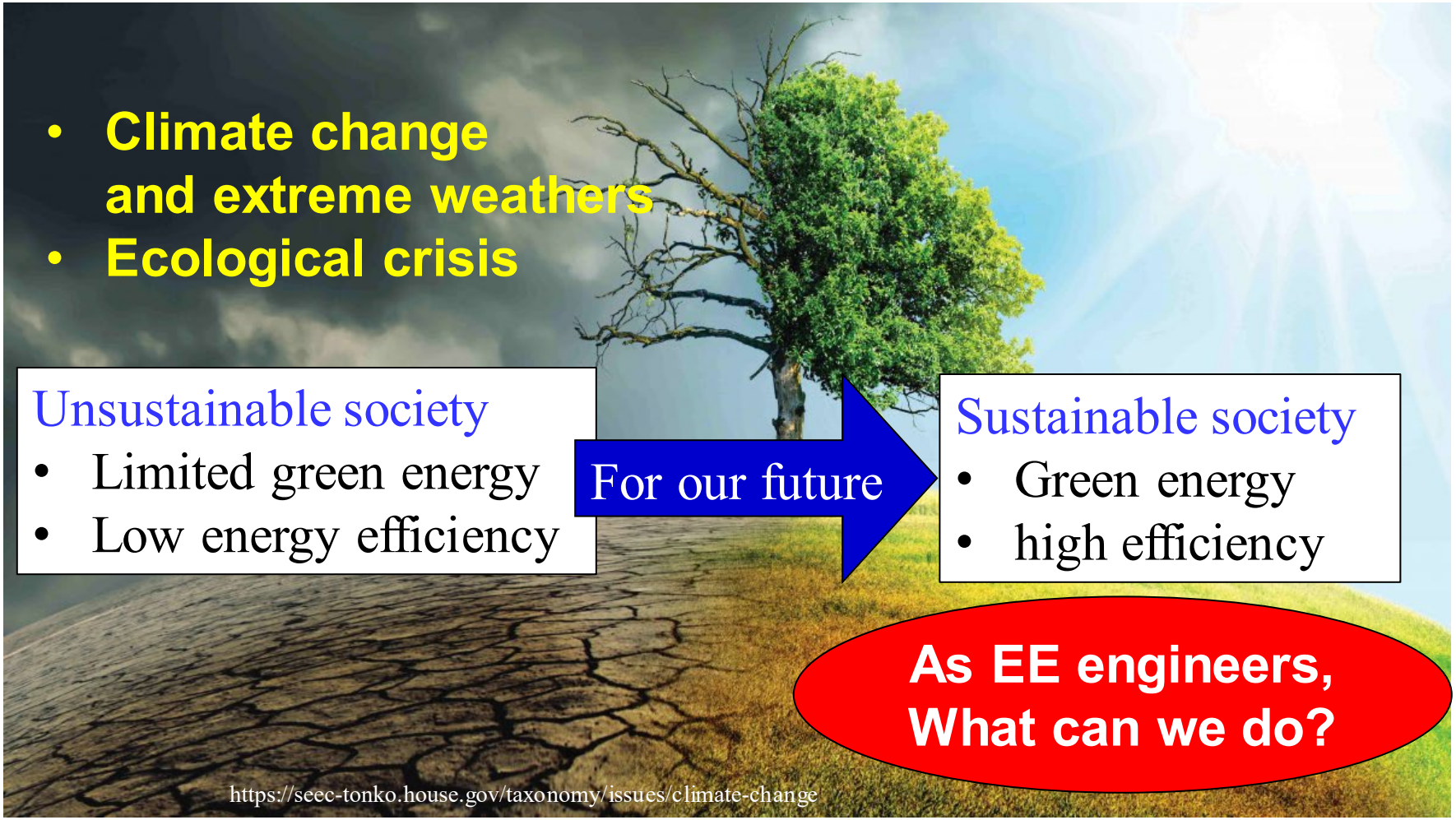




- ✓ **Metals**: Ag, Pd, Te
- ✓ **Methods**:
  Ebeam evaporation,
  Molecular beam epitaxy

Uniform High-Aspect-Ratio GaN Vertical Sub-30-nm-Diameter Nanowires Formed by Optimized Two-Step Etching Process

Pao-Chuan Shih (pcshih@mit.edu) and Tomás Palacios



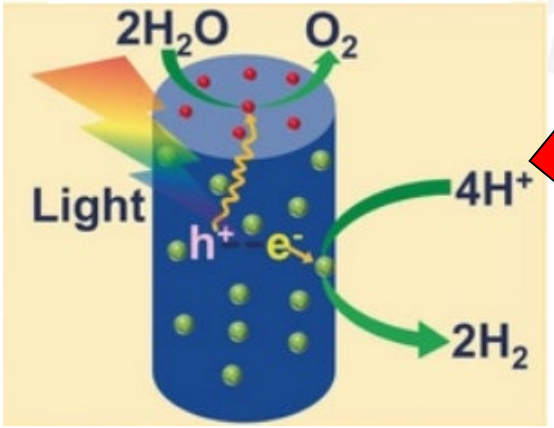
Uniform High-Aspect-Ratio GaN Vertical Sub-30-nm-Diameter Nanowires Formed by Optimized Two-Step Etching Process

Pao-Chuan Shih (pcshih@mit.edu) and Tomás Palacios

As EE engineers, What can we do?

GaN

Green energy

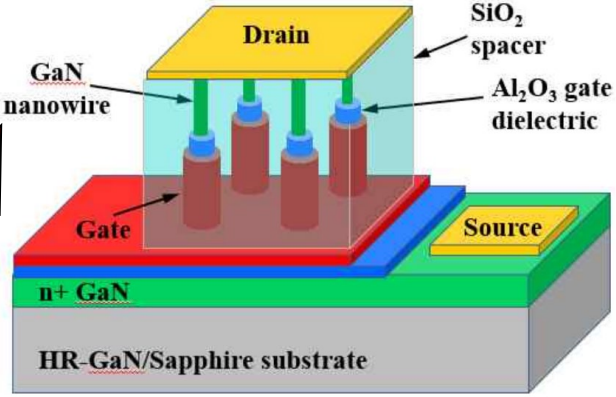


https://doi.org/10.1002/anie.201912844

Solar-induced H_2 fuel generation

https://www.cnet.com/tech/home-entertainment/wall-sized-million-dollar-microled-tvs-point-to-the-future-of-television/

Efficient micro-LEDs



10.1109/DRC.2015.7175539

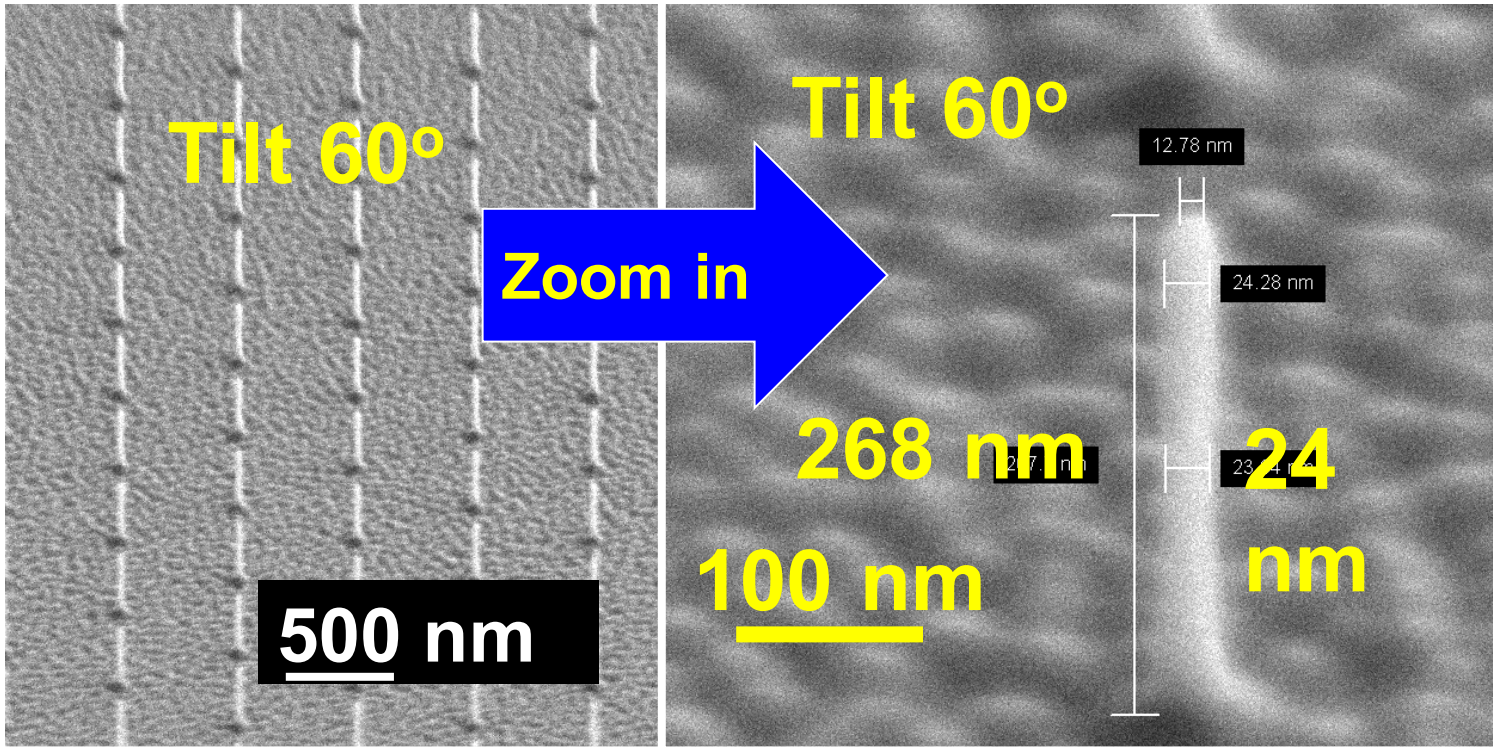
Power electronics

Uniform High-Aspect-Ratio GaN Vertical Sub-30-nm-Diameter Nanowires Formed by Optimized Two-Step Etching Process

Pao-Chuan Shih (pcshih@mit.edu) and Tomás Palacios

To achieve these…

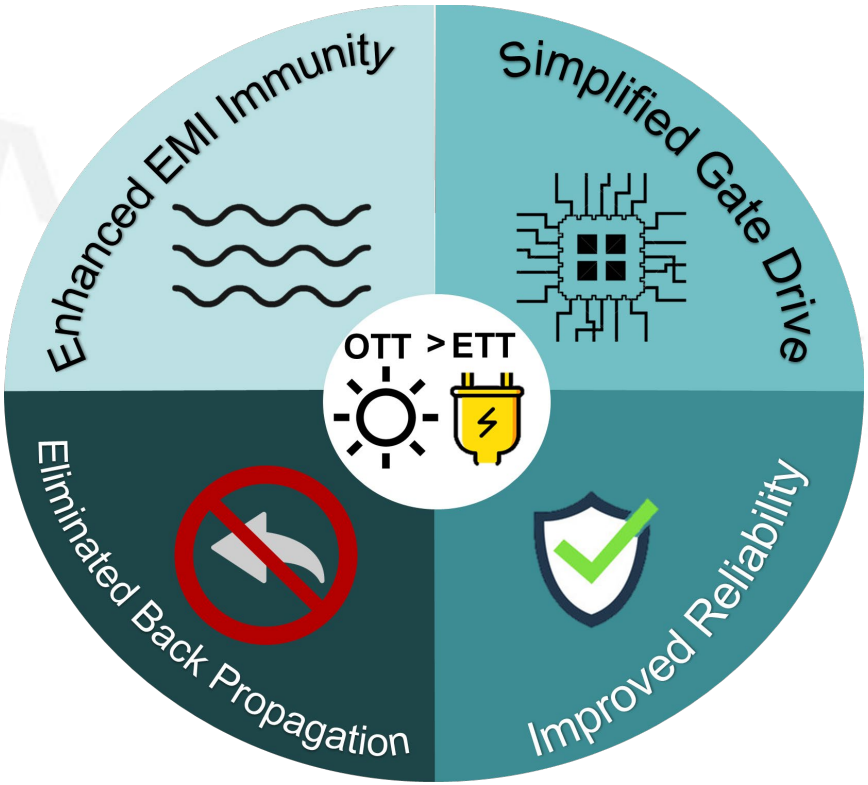
Technologies to form uniform GaN nanostructures is critical



Optically Controlled Vertical GaN Power finFET

Jung-Han Hsia, Kevin Limanta, Joshua Perozek, Richard Molnar and Tomás Palacios

Sponsor: Office of Naval Research



Optically Controlled Vertical GaN Power finFET

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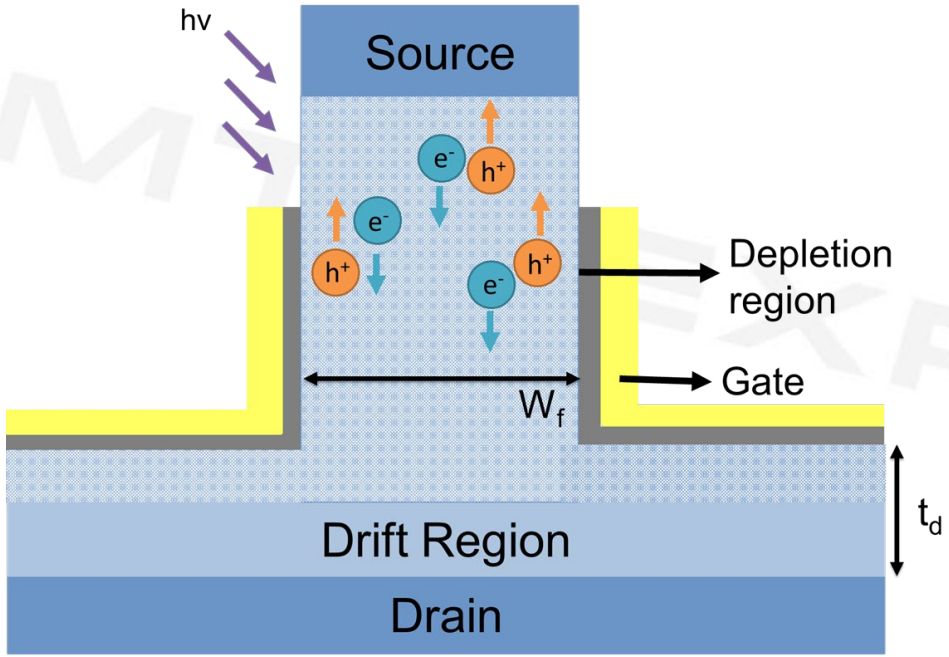


* Not drawn to scale

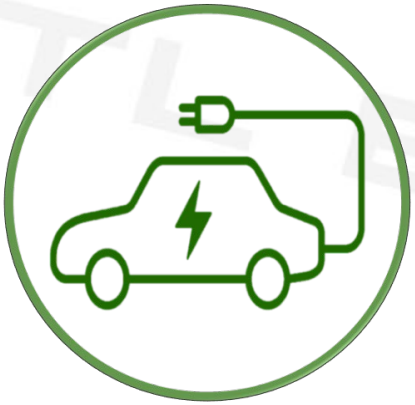
Optically Controlled Vertical GaN Power finFET

Jung-Han Hsia, Kevin Limanta, Joshua Perozek, Richard Molnar and Tomás Palacios

Sponsor: Office of Naval Research

Smart Grid

Electric Vehicle

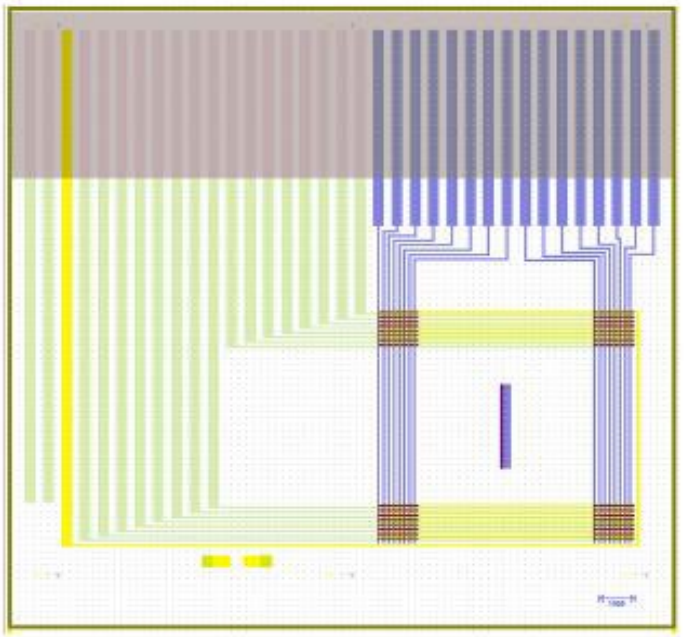


Pulsed Power

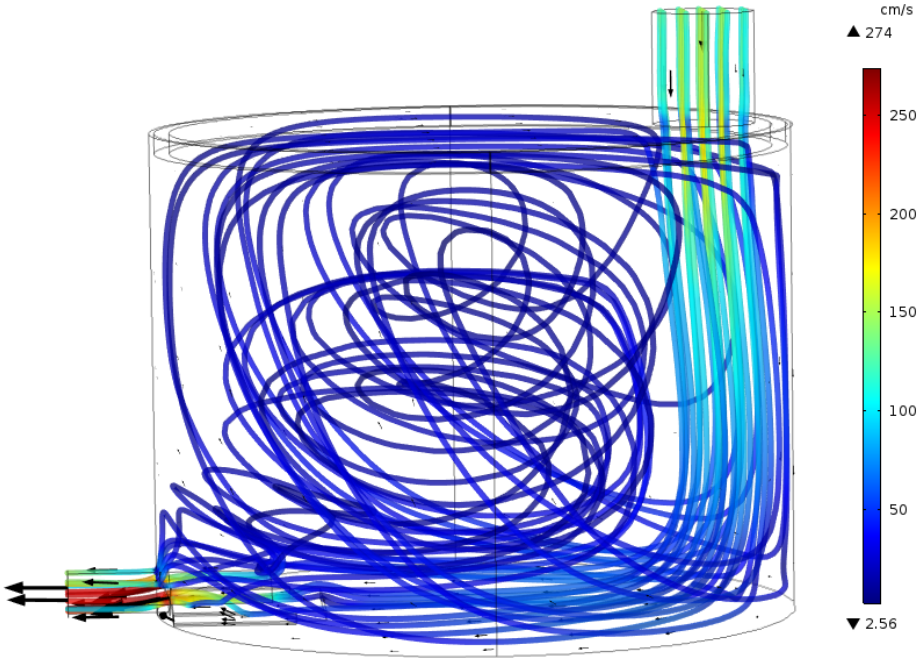
S3.6 Chamber Design of a Portable Breathalyzer for Disease Diagnosis

D. Morales, M. Xue, T. Palacios

Patient → Breath → Device → Processing → Diagnosis



Sensor to analyze the volatile organic compounds



Fluid mechanics simulations

Integration and Evaluation of SiN and Al_2O_3 as Passivation and Gate-dielectrics in GaN HEMTs

G. Micale[1,2], R. Ley[2], T. Palacios[1], B. Briggs[2]

[1]Microsystems Technology Laboratories, MIT

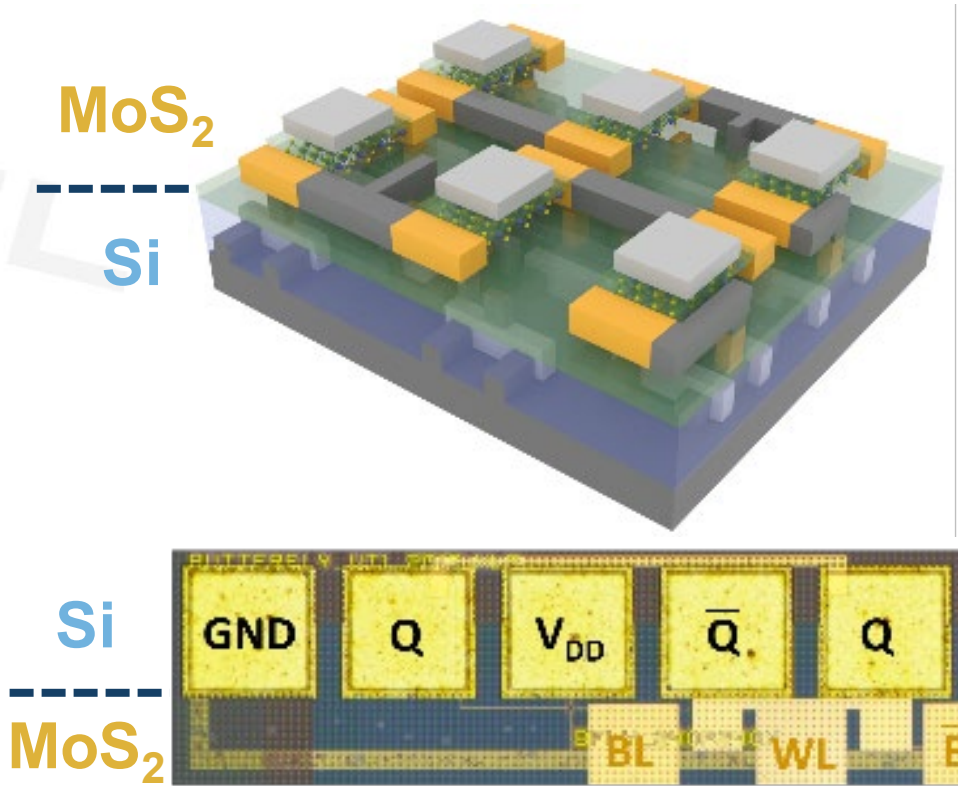
[2]Applied Materials

Low-temperature Synthesis of Monolayer MoS_2 on 200-mm Silicon Platform

Jiadi Zhu, Ji-Hoon Park, Steven A. Vitale, Jiangtao Wang, Mohamed Mohamed, Tianyi Zhang, Mantian Xue, Xudong Zheng, Zhien Wang, Jing Kong, Tomás Palacios

Growth @ 275 °C

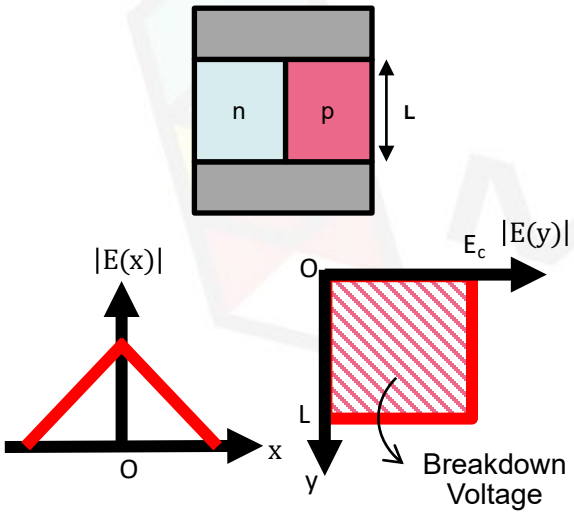
MoS_2 on Si CMOS circuit

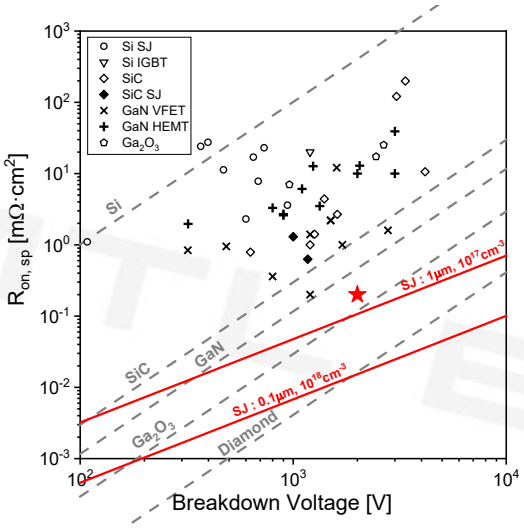


Use of Ion Implantation to Engineer the Electric Field Profiles in GaN Superjunctions

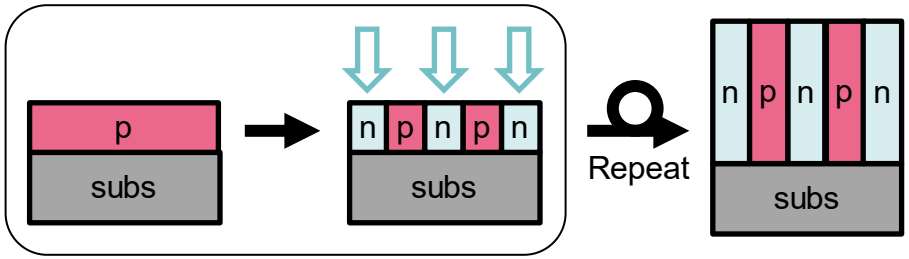
Minsik Oh, Prof. Tomas Palacios

GaN Superjunction Devices

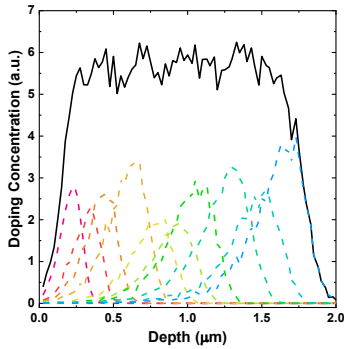




Multiepitaxy & Ion Implantation

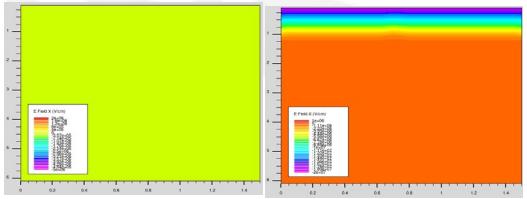


Ion Implantation Simulation

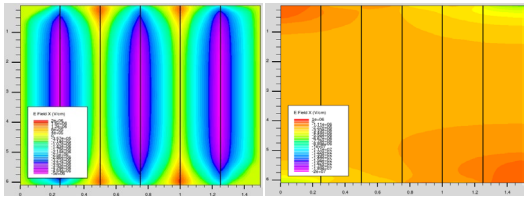


E-field Profile Simulation

[N-type Drift Layer]

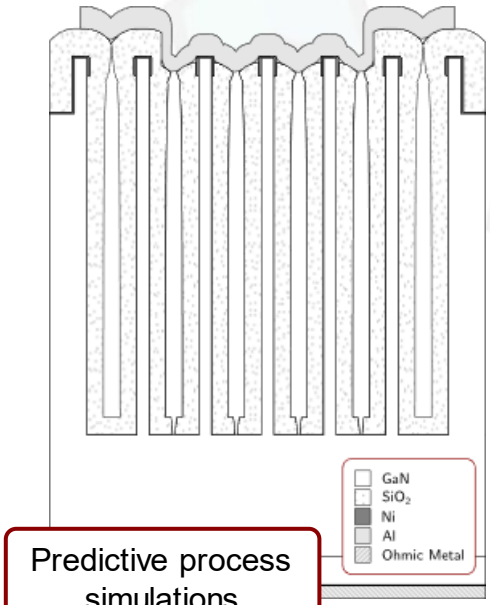


[SJ Drift Layer]

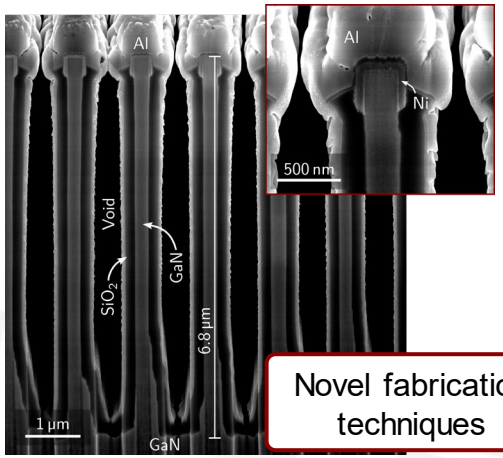


Vertical GaN Superjunctions

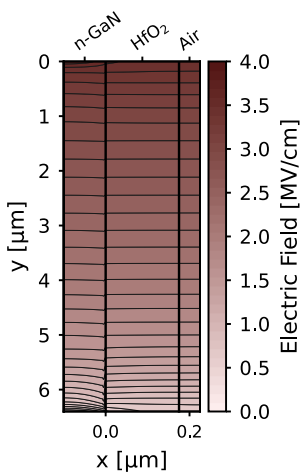
Joshua Perozek and Tomás Palacios

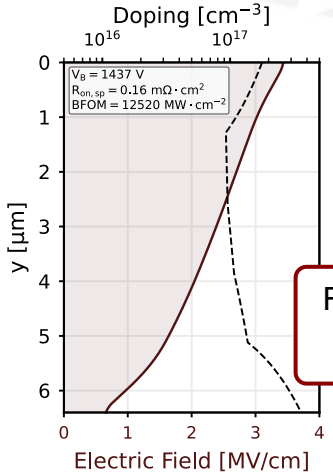


Predictive process simulations

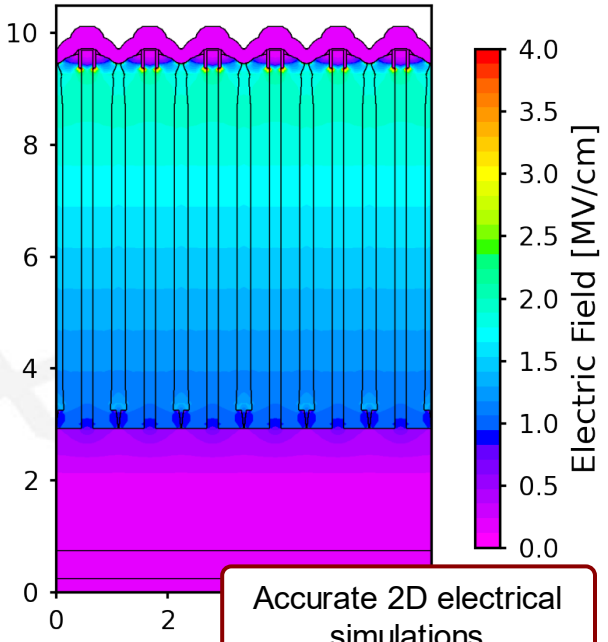


Novel fabrication techniques





Robust design optimization



Accurate 2D electrical simulations

High-power AlGaN finFET for mm-Wave applications

Hridibrata Pal, Pao-Chuan Shih, Tomás Palacios, hpal@mit.edu

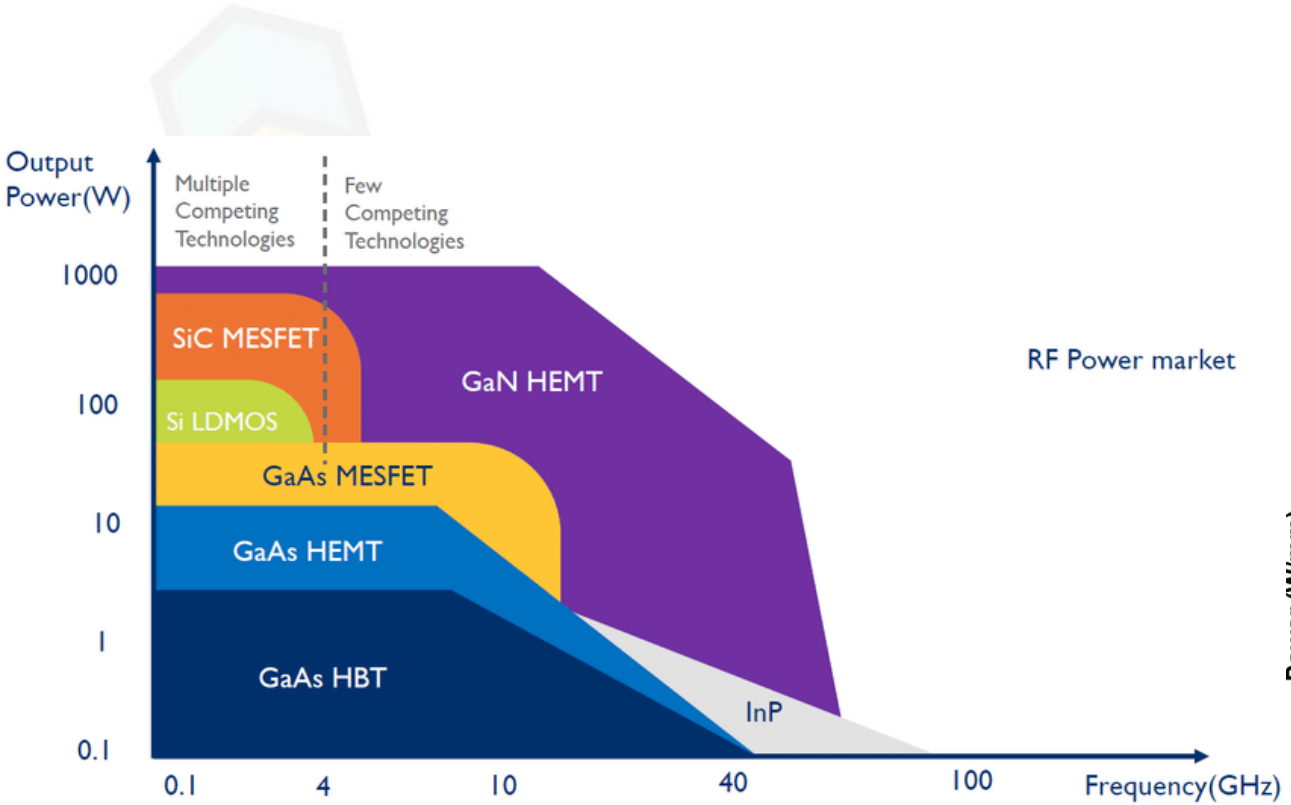
How can it be achieved?

Efficient power amplifier is the key

Acknowledgement: US Army Research Office

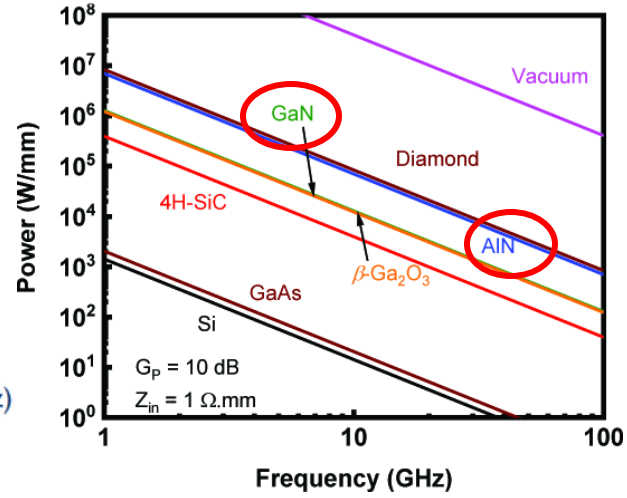
High-power AlGaN finFET for mm-wave applications

Hridibrata Pal, Pao-Chuan Shih, Tomás Palacios, hpal@mit.edu



Next hero semiconductor

High Al-AlGaN



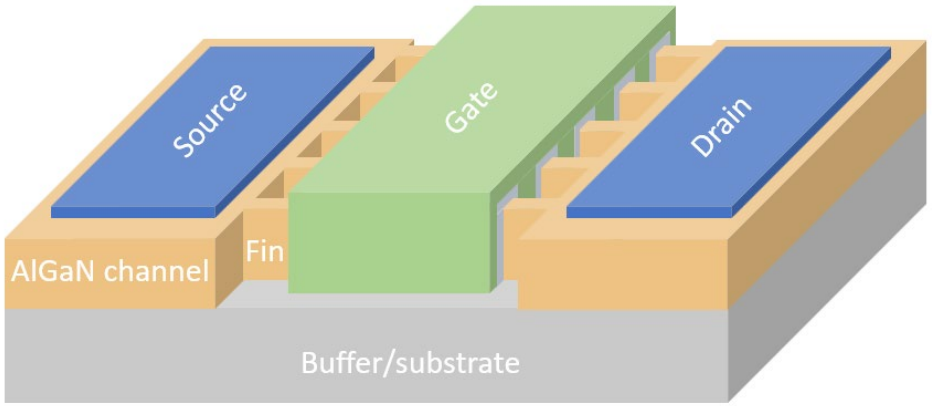
Acknowledgement: US Army Research Office

High-power AlGaN finFET for mm-wave applications

Hridibrata Pal, Pao-Chuan Shih, Tomás Palacios, hpal@mit.edu

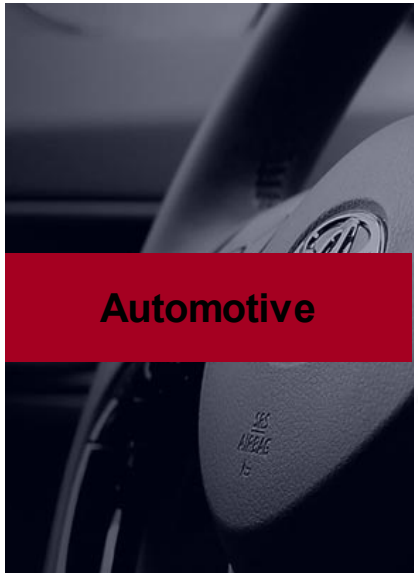
$Al_{0.7}Ga_{0.3}N$ finFET with high aspect ratio fins

higher power density

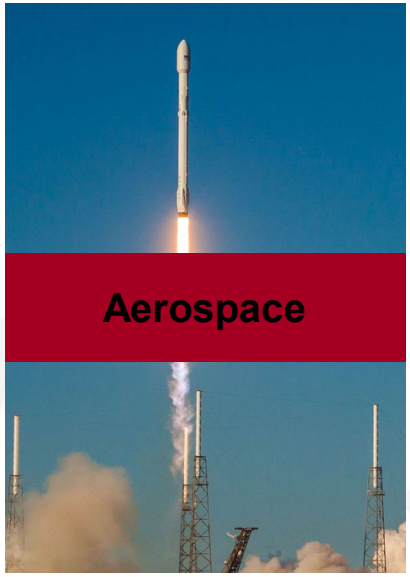


Acknowledgement: US Army Research Office

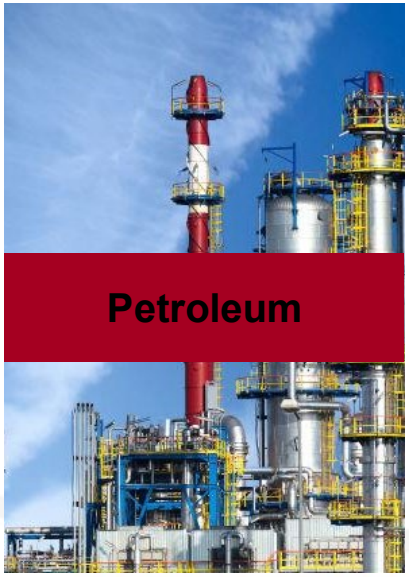
Robust High Temperature Electronics with AlGaN/GaN HEMT Technologies



Automotive



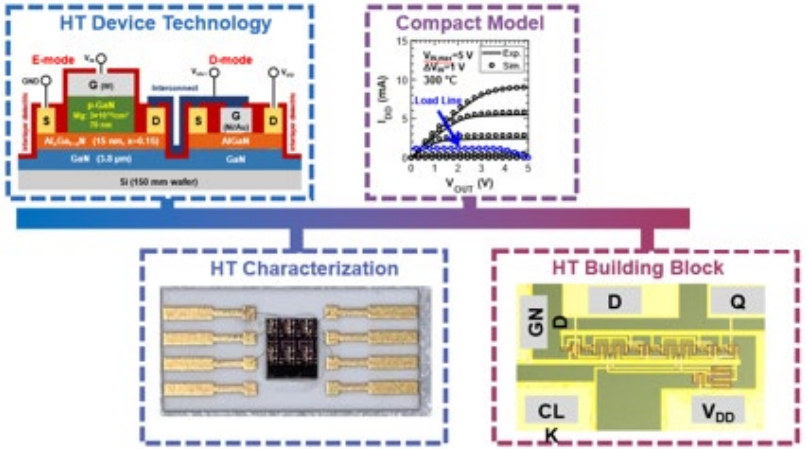
Aerospace



Petroleum

Geothermal

Require digital, power, and RF electronics working at 500° C and beyond!



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Congratulations !!

We are SiMpLy Awesome!!